REMARKS

This application has been carefully reviewed in light of the Office Action dated August 3, 2007. Claims 1, 3 to 7, 20, 22 to 26 and 39 remain in the application, with Claims 2, 8 to 19, 21, 27 to 38 and 40 to 61 having been withdrawn. Claims 1, 20 and 39 are the independent claims. Reconsideration and further examination are respectfully requested.

Claims 8 to 19, 27 to 38 and 40 to 61 were withdrawn from further consideration due to the restriction requirement. Without conceding the correctness of the restriction requirement, the withdrawn claims have nonetheless been cancelled so as to place the application in better condition for allowance.

Claim 39 was rejected under 35 U.S.C. § 101. Without conceding the correctness of the rejection, the preamble of Claim 39 has been amended to make it even clearer as to the statutory subject matter of the invention. Reconsideration and withdrawal of the rejection are respectfully requested.

Claims 1 to 7, 20 to 26 and 39 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,977,756 (Nakano) in view of U.S. Patent No. 6,956,674 (Ishikawa). Reconsideration and withdrawal of the rejections are respectfully requested.

The present invention aims to reduce the necessary memory for processing image data by dividing input image data, that is corrected by a quantization error, into a decimal portion (lower bits) and an integral portion (upper bits), wherein only the integral portion of image data is buffered. Further, the image quality of a highlight portion can be increased since the decimal portion at the error diffusion calculation is bit connected to the

image data as the lower bits of it and decimal portion of a correction value is diffused without truncation.

Referring specifically to the claims, amended independent Claim 1 is directed to an image processing apparatus comprising a bit connection component that connects a cumulative value of decimals of preceding image data to input image data as lower bits of the input image data, a correction component that corrects the connected input image data with a quantization error, a latch component that latches a decimal portion of the corrected input image data, a quantization component that quantizes an integral portion of the corrected input image data, a calculation component that calculates the quantization error, which is generated by quantization by the quantization component, to provide the calculated quantization error to the correction component, a buffer that stores the calculated quantization error, and an error diffusion component that diffuses the quantization error on the basis of at least a quantization error of a first pixel, which is stored in the buffer.

Claims 20 and 39 are method and computer medium claims, respectively, that substantially correspond to Claim 1.

The applied art, alone or in any permissible combination, is not seen to disclose or to suggest the features of Claims 1, 20 and 39, and in particular, is not seen to disclose or to suggest at least the features of a bit connection component (step) that connects a cumulative value of decimals of preceding image data to input image data as lower bits of the input image data, a quantization component (step) that quantizes an integral portion of the corrected input image data, a calculation component that calculates a quantization error, which is generated by quantization by the quantization component

(step), to provide the calculated quantization error to a correction component, and a buffer that stores the calculated quantization error.

Nakano is seen to disclose that a data driven type processing device has an error diffusion computing unit built therein. An error holding register is provided within the error diffusion-computing unit, and is used to successively store and update a value of error information of a pixel that is to be diffused to a neighboring pixel being processed continuously. An error data memory is provided outside the computing unit, and is used to store and update a value of the error information that is to be diffused to another neighboring pixel being processed discontinuously. The error information and the values to be diffused are stored in a packet, and the packet is circulated for operation. However, Nakano is not seen to disclose or to suggest at least the features of a bit connection component (step) that connects a cumulative value of decimals of preceding image data to input image data as lower bits of the input image data, a quantization component (step) that quantizes an integral portion of the corrected input image data, a calculation component that calculates a quantization error, which is generated by quantization by the quantization component (step), to provide the calculated quantization error to a correction component, and a buffer that stores the calculated quantization error.

Ishikawa is seen to disclose that an image processor employing error diffusion is provided with a multi-valued dithering part, for reducing the bit number of computing in a feedback loop for errors. Thus, an operation can be performed at a high speed while the capacity of an error storage memory can be reduced. However, Ishikawa, like Nakano, is not seen to disclose or to suggest at least the features of a bit connection component (step) that connects a cumulative value of decimals of preceding image data to

input image data as lower bits of the input image data, a quantization component (step) that quantizes an integral portion of the corrected input image data, a calculation component that calculates a quantization error, which is generated by quantization by the quantization component (step), to provide the calculated quantization error to a correction

In view of the foregoing amendments and the deficiencies of the applied art, Claims 1, 20 and 39, as well as the claims dependent therefrom, are believed to be in condition for allowance.

No other matters having been raised, the entire application is believed to be in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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